

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Hidemasa ZAMA, et al.

FILING DATE: Herewith

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT, LOGIC OPERATION CIRCUIT, AND FLIP FLOP

**LIST OF INVENTORS' NAMES AND ADDRESSES**

ASSISTANT COMMISSIONER FOR PATENTS  
WASHINGTON, D.C. 20231

SIR:

Listed below are the names and addresses of the inventors for the above-identified patent application.

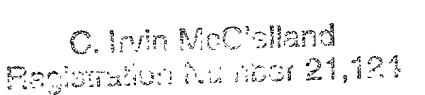
Hidemasa ZAMA	Kawasaki-shi, Japan
Masayuki KOIZUMI	Yokohama-shi, Japan
Yukiko ITO	Yokosuka-shi, Japan
Kimiyoshi USAMI	Yokohama-shi, Japan
Naoyuki KAWABE	Kawasaki-shi, Japan
Masahiro KANAZAWA	Yokohama-shi, Japan
Toshiyuki FURUSAWA	Tokyo-TO, Japan

A declaration containing all the necessary information will be submitted at a later date.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER & NEUSTADT, P.C.

  
\_\_\_\_\_  
Marvin J. Spivak  
Registration No. 24,913

  
\_\_\_\_\_  
C. Irvin McClelland  
Registration Number 21,124



**22850**

Tel. (703) 413-3000  
Fax. (703) 413-2220  
(OSMMN 11/98)